UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,196	03/25/2004	Brian Holscher	TRAN-P247	8666

7590 06/23/2008

WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
GU, SHAWN X	
ART UNIT	PAPER NUMBER
2189	

MAIL DATE	DELIVERY MODE
06/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,196	HOLSCHER ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed on 29 February 2008. Claims 1-20 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-11, 13-15 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Moreno et al. [US 6,678,795 B1] (hereinafter "Moreno").

Per claims 1, 9, and 18, Moreno teaches a request tracking data prefetch apparatus (Fig 2, combination of 204 Li, 254 Lj, 206 CCi, 256 CCj, 282 PUM Table, 284 Prefetch Engine) for a computer system (the system in Fig 2), comprising:

a processor (Fig 2, 252 Pj);

a system memory (Fig 2, 270 Memory) coupled to the processor;

a prefetch unit (Fig 2, combination of 290 PUM Engine and 256 CCj; Col 5, Lines 56-58) coupled to the system memory;

a plurality of trackers (PUM Entries; Col 4, Lines 45-57) included in the prefetch unit, wherein the trackers are respectively configured to recognize an access to a plurality of cache lines and accesses to pages of the system memory by a processor of the computer system (Col 4, Lines 45-57; Col 5, Lines 58-67; Col 7, Lines 1-7; also presented by the rows of Fig 1's table), and configured to recognize accesses to cache lines (by searching and identifying the cache lines with their corresponding bits set to "1" in the PUM entry; see Fig. 1) that form a stream type access pattern (see col.1, lines 63-67, col.2, lines 1-2 and col.6, lines 56-67 and col.7, lines 1-3; also see Fig. 1); and

a cache memory (Fig 2, 254 Lj) coupled to the prefetch unit, wherein the prefetch unit uses a bit vector (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) to predictively load target cache lines from the system memory into the cache memory (Col 4, Lines 58-67; Col 5, Lines 1-2) to reduce an access latency of the processor (Col 4, Lines 36-44), and wherein the target cache lines are indicated by the stream type access pattern identified by the trackers (see col.1, lines 63-67, col.2, lines 1-2, col. 6, lines 56-67 and col. 7, lines 1-3; also see Fig. 1).

It is clear claim 1's apparatus for a computer system is already described by the apparatus of claim 9, and the high latency memory and low latency memory of claim 1 respectively correspond to the system memory and cache memory of claim 9.

It is also clear that the method of claim 18 is performed by the apparatus of claim 9, as the bit vector of claim 9 clearly tracks multiple data transfer patterns (as clearly indicated by the cache line access history patterns displayed by the rows of Fig 1) between the high latency memory/system memory and the lower latency memory/cache memory.

Per claims 2 and 10, Moreno further teaches each of the trackers include a tag (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) configured to recognize accesses to corresponding cache lines of the high latency memory by the processor.

Per claims 3 and 11, Moreno further teaches a plurality of system memory accesses by the processor to the high latency memory as recognized by the tag are used by the trackers to determine the target cache line for a predictive load into the cache memory/low latency memory (Col 7, Lines 4-10 and Lines 28-63).

Per claim 5, Moreno further teaches the high latency memory comprises a memory block of a plurality of memory blocks of the computer system (pages; Col 4, Lines 36-44).

Per claims 6 and 13, Moreno further teaches the system/high latency memory comprises a plurality of 4KB pages (Col 4, Lines 36-44; Col 5, Lines 11-14), and the memory block comprises a four kilobyte page (a memory block is a 4KB page).

Per claims 7 and 14, Moreno further teaches each of the plurality of trackers includes a tag configured to monitor a sub portion of the high latency memory block/page for accesses by the processor (a portion of the PUM entry bits which indicate cache line accesses of a page, in other words; Col 4, Lines 45-57; Col 5, Lines 3-22; since access to every cache line of a page is represented by a corresponding bit in the PUM entry, a portion of those bits monitor a sub portion of a page for accesses).

Per claim 8, Moreno further teaches the high latency memory is a system memory (Fig 2, 270 Memory; Col 5, Lines 36-55; Memory 270 is main memory of computer system 200) of the computer system.

Per claim 15, Moreno further teaches the cache lines 128 byte cache lines (Col 5, Lines 12-14) and wherein a tag (half of the PUM entry bits which indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) is used to monitor half of a page (since access to every cache line of a page is represented by a corresponding bit

in the PUM entry, half of those bits monitor half of a page) for accesses by the processor.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno et al. [US 6,678,795 B1] (hereinafter “Moreno”).

Per claims 4, 12, and 20, Moreno further teaches accesses by the processor to adjacent cache lines of a page (Fig 1, rows with adjacent “1”s) of the system memory are used to determined the target cache line of a stream type access pattern for a predictive load into the cache memory, wherein the adjacent cache lines have adjacent addresses (Col 4, Lines 45-57; Col 5, Lines 3-22; Col 7, Lines 4-10 and Lines 28-63).

Moreno does not specifically teach that these accesses are consecutive. However, in Moreno's Fig 1, rows with Indexes 184772, 1502531, 1502688 all indicate 2 or 3 total page accesses to a page with only 2 adjacent cache lines indicated as accessed, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant invention that objects or programs bigger than a cache line (128 bytes) are stored in more than one adjacent cache lines of the same page, and when they are requested by the processor, these cache lines will be accessed consecutively by the processor. For instance, if an object between the size of 129 bytes and 256 bytes is stored in the page with index 184772, then a request by the processor for this object would result in consecutive accesses to the two adjacent cache lines storing the object, and these accesses are used by Moreno's invention to determine the target cache line for a predictive load into the cache memory. Furthermore, Moreno also teaches these accesses are consecutive as set forth above in claims 1, 9 and 18 (stream type cache line access pattern).

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Bittel et al. [US 6,820,173 B1] (hereinafter "Bittel").

Per claim 16, Moreno already substantially discloses the claim as described above, but does not specifically disclose that the cache memory is a prefetch cache memory within the prefetch unit. However, Bittel teaches a prefetch apparatus (Fig 7) comprising a prefetch unit (Fig 3, 208 Prefetcher), and a cache memory (Fig 3, 306

Cache) within the prefetch unit. It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Bittel's cache memory in Moreno's prefetch unit in order to further increase caching capacity of the system while allow the existing caches (L1, L2, etc) to serve their original purposes, furthermore by using an internal cache of the prefetcher instead of the L1 cache, there is no additional interconnection wiring required between the prefetcher and the L1 cache.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Microsoft Computer Dictionary (hereinafter "Microsoft").

Per claim 17, Moreno already substantially discloses the claim as described above, and further teaches the cache memory is an L1 cache memory (Col 5, Lines 12-13), but does not specifically disclose that the cache memory is an L2 cache memory. However, Microsoft discloses that a typical L2 cache has bigger capacity than a typical L1 (Page 304), and therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make Moreno's cache memory a L2 cache instead of a L1 cache in order to have larger caching capacity.

8. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Brooks [6,081,868] (hereinafter "Brooks").

Per claim 19, Moreno already substantially discloses the claim as described above, and further teaches the computer system includes a plurality of processors (Fig 2, 202 Pi and 252 Pj), and wherein each of the processors is coupled to a respective lower latency memory (Fig 2, 204 Li and 254 Lj) and are all coupled to a high latency memory (Fig 2, 270 Memory), but does not specifically disclose that each of the processors is coupled to a respective high latency memory. However, Brooks teaches a prefetch system wherein each of a plurality of processors is coupled to a respective high latency memory (Brooks: Fig 2, a CPU is coupled to a CPU private memory in each CPU block; CPU Private Memory has higher latency than CPU Cache), in order to provide data storage exclusively for the associated CPU (Brooks: Col 5, Lines 25-30). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make each of Moreno's plurality of processors to be coupled to a respective high latency memory in order to provide data storage exclusively for the associated processor.

Response to Arguments

9. Applicant's arguments with respect to claims 1-20 have been fully considered but are not persuasive.

Regarding the Applicant's argument that Moreno does not teach or suggest the portion of claim 9 including the limitation "the target cache lines are indicated by the stream type access pattern" (see Remarks filed 29 February 2008, pages 1-3), the Applicant appears to rely on the assertion that "Moreno does not specifically disclose

that the order of previous accesses to the two cache lines was not interrupted by other cache line accesses" (see Remarks, page 2, first paragraph) and that Moreno teaches away from the claimed invention by "generating prefetch requests based solely on each cache line bit set to 1", thereby resulting "in each request being based any access pattern which is substantially different from stream type access as claimed" (see Remarks, page 3, last paragraph). Therefore, it appears the Applicant agrees that Moreno teaches the target caches lines are indicated/identified by the trackers, but disagrees that the indication/identification of the target cache lines is related to any stream type access pattern identified by the trackers.

However, none of the pending claims clearly define what is and what is not considered a stream-type access pattern. The Applicant's disclosure on page 9, lines 5-14 explains accesses to cache lines x, then x+1, x+2, and so on may be taken as a stream-type-sequential access pattern. The disclosure further explains on page 11, lines 14-19 that a stream-type access is recognized when indicators of adjacent cache lines show that the adjacent cache lines have been accessed. Page 11, line 18 of the disclosure also describes "a sequential decrementing stream-type access".

The Examiner would like to remind the Applicant that the pending claims only recite "stream type access pattern" while the specification teaches "sequential stream-type access pattern". These two terms have clearly different scopes and meanings and therefore cannot be used to replace each other in the context of claim interpretation. Therefore, the claimed "stream-type access pattern" is not clearly defined and the Examiner broadly interpreted it to constitute any access pattern that result in adjacent

cache lines being accessed in any order, which is a feature taught by Moreno as set forth above in the rejection of claims 1, 9 and 18. The Examiner also respectfully reminds the Applicant that the Applicant's own disclosure clearly teaches that the recognizing of a stream-type access is achieved by showing in indicators of adjacent cache lines that the adjacent cache lines have been accessed (see specification, page 11, lines 14-19), and Moreno's tracker shown in Fig. 1 clearly demonstrate this capability. There is no additional teaching by the Applicant on how the adjacent cache lines are accessed in order to constitute a stream-type access pattern. In other words, if the recognizing is merely a showing of adjacent cache lines being accessed, then Moreno can recognize a stream-type access as defined by the Applicant by Moreno's teaching in Fig. 1. The fact that Moreno does not limit its teaching to the prediction and prefetching of cache lines identified by a sequential pattern (see Moreno, col. 1, lines 63-67) is not an indication that it teaches away from the claimed invention. Not limiting one's teaching to a particular feature is not equivalent to a teaching that is mutually exclusive to that particular feature.

Regarding the Applicant's argument that the combination of Moreno and Bittel does not render claim 16 obvious because "the northbridge of Bittel is located between the DRAM and the processor and is coupled to the processor by the system bus" and "Bittel teaches a prefetch unit not configured or coupled to observe access to L1 and L2 caches" (see Remarks, page 4, last paragraph to page 5, first paragraph), the Applicant is respectfully reminded that claim 16 does not recite the prefetch unit is configured to

coupled to observe access to L1 and L2 caches and it appears the Applicant is attempting to bring in teachings only disclosed in the specification but not specifically claimed into the claim language. The structural limitations in claim 16 describe that the prefetch unit is coupled to the system memory, which is in turn coupled to the processor, and the cache memory is within the prefetch unit. The term "couple" can be reasonably and broadly interpreted as direct or indirect connection by one of ordinary skill. By the Applicant's on admission, Bittel's prefetcher is coupled to the processor, and Fig. 7 in Bittel also shows that the prefetcher is coupled to a system memory/DRAM and the DRAM is coupled to the processor by its indirect connection to CPU2MCM through the prefetcher 208. Bittel also shows in Fig. 7 that the cache memory 306 is within the prefetcher 208.

Regarding the Applicant's argument that the combination of Moreno and Microsoft renders claim 17 obvious (see Remarks, page 5, last paragraph to page 6, first paragraph), the Examiner would like to clarify the statement "Microsoft teaches a typical L2 cache has bigger capacity than a typical L1 cache". What should be clear is that a typical L2 cache has bigger capacity than a typical L1 cache on the same processor is a well-known concept in the state of the art. It should be noted also that Microsoft does not limit its teaching to the i486 processor alone, but states the L1 cache is built into i486 and higher-level processors and typically contains 8 KB and the L2 cache is on a motherboard that uses an i486 or higher-level processor and typically contains 128 KB to 1 MB. Therefore, Microsoft clearly demonstrates a L2 cache built

for a processor has a bigger capacity than a L1 cache on the same processor and the motivation for combining Moreno and Microsoft is reasonable and clearly set forth above in the rejection of claim 17.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/SHAWN X GU/

Shawn X Gu
Patent Examiner
Art Unit 2189

19 June 2008

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189